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| **Project Status (10/14/2015 - 23:34:01)** | | | |
| **Project File:** | system.xmp | **Implementation State:** | Programming File Generated |
| **Module Name:** | system | * **Errors:** |  |
| **Product Version:** | EDK 14.4 | * **Warnings:** |  |

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| **XPS Reports** | | | | | **[-]** |
| **Report Name** | **Generated** | **Errors** | **Warnings** | **Infos** | |
| Platgen Log File | Wed 14. Oct 22:55:59 2015 | 0 | 6 Warnings (0 new) | 14 Infos (2 new) | |
| Simgen Log File |  |  |  |  | |
| BitInit Log File |  |  |  |  | |
| System Log File | Wed 14. Oct 23:29:24 2015 |  |  |  | |

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| **XPS Synthesis Summary (estimated values)** | | | | | | **[-]** |
| **Report** | **Generated** | **Flip Flops Used** | **LUTs Used** | **BRAMS Used** | **Errors** | |
| system | Wed 14. Oct 22:56:52 2015 | 4126 | 7516 | 2 | 0 | |
| system\_audio\_project\_0\_wrapper | Wed 14. Oct 22:55:58 2015 | 3572 | 6771 | 2 | 0 | |
| system\_i2s\_ctrl\_0\_wrapper | Wed 14. Oct 22:48:55 2015 | 291 | 242 |  | 0 | |
| system\_axi\_interconnect\_1\_wrapper | Sun 11. Oct 22:11:54 2015 | 158 | 297 |  | 0 | |
| system\_oled\_bypass\_ps2pl\_0\_wrapper | Tue 29. Sep 10:12:01 2015 | 79 | 83 |  | 0 | |
| system\_axi\_gpio\_0\_wrapper | Tue 29. Sep 10:11:29 2015 | 26 | 34 |  | 0 | |
| system\_processing\_system7\_0\_wrapper | Tue 29. Sep 10:09:31 2015 |  | 89 |  | 0 | |

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| **Device Utilization Summary (actual values)** | | | | | **[-]** |
| **Slice Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Registers | 4,109 | 106,400 | 3% |  | |
| Number used as Flip Flops | 4,051 |  |  |  | |
| Number used as Latches | 0 |  |  |  | |
| Number used as Latch-thrus | 0 |  |  |  | |
| Number used as AND/OR logics | 58 |  |  |  | |
| Number of Slice LUTs | 7,035 | 53,200 | 13% |  | |
| Number used as logic | 6,220 | 53,200 | 11% |  | |
| Number using O6 output only | 5,679 |  |  |  | |
| Number using O5 output only | 24 |  |  |  | |
| Number using O5 and O6 | 517 |  |  |  | |
| Number used as ROM | 0 |  |  |  | |
| Number used as Memory | 710 | 17,400 | 4% |  | |
| Number used as Dual Port RAM | 584 |  |  |  | |
| Number using O6 output only | 584 |  |  |  | |
| Number using O5 output only | 0 |  |  |  | |
| Number using O5 and O6 | 0 |  |  |  | |
| Number used as Single Port RAM | 0 |  |  |  | |
| Number used as Shift Register | 126 |  |  |  | |
| Number using O6 output only | 56 |  |  |  | |
| Number using O5 output only | 0 |  |  |  | |
| Number using O5 and O6 | 70 |  |  |  | |
| Number used exclusively as route-thrus | 105 |  |  |  | |
| Number with same-slice register load | 99 |  |  |  | |
| Number with same-slice carry load | 4 |  |  |  | |
| Number with other load | 2 |  |  |  | |
| Number of occupied Slices | 2,756 | 13,300 | 20% |  | |
| Number of LUT Flip Flop pairs used | 7,563 |  |  |  | |
| Number with an unused Flip Flop | 3,724 | 7,563 | 49% |  | |
| Number with an unused LUT | 528 | 7,563 | 6% |  | |
| Number of fully used LUT-FF pairs | 3,311 | 7,563 | 43% |  | |
| Number of unique control sets | 220 |  |  |  | |
| Number of slice register sites lost to control set restrictions | 945 | 106,400 | 1% |  | |
| Number of bonded IOBs | 15 | 200 | 7% |  | |
| Number of LOCed IOBs | 15 | 15 | 100% |  | |
| Number of bonded IOPAD | 130 | 130 | 100% |  | |
| IOB Flip Flops | 3 |  |  |  | |
| Number of RAMB36E1/FIFO36E1s | 0 | 140 | 0% |  | |
| Number of RAMB18E1/FIFO18E1s | 3 | 280 | 1% |  | |
| Number using RAMB18E1 only | 3 |  |  |  | |
| Number using FIFO18E1 only | 0 |  |  |  | |
| Number of BUFG/BUFGCTRLs | 2 | 32 | 6% |  | |
| Number used as BUFGs | 2 |  |  |  | |
| Number used as BUFGCTRLs | 0 |  |  |  | |
| Number of IDELAYE2/IDELAYE2\_FINEDELAYs | 0 | 200 | 0% |  | |
| Number of ILOGICE2/ILOGICE3/ISERDESE2s | 1 | 200 | 1% |  | |
| Number used as ILOGICE2s | 1 |  |  |  | |
| Number used as ILOGICE3s | 0 |  |  |  | |
| Number used as ISERDESE2s | 0 |  |  |  | |
| Number of ODELAYE2/ODELAYE2\_FINEDELAYs | 0 |  |  |  | |
| Number of OLOGICE2/OLOGICE3/OSERDESE2s | 4 | 200 | 2% |  | |
| Number used as OLOGICE2s | 4 |  |  |  | |
| Number used as OLOGICE3s | 0 |  |  |  | |
| Number used as OSERDESE2s | 0 |  |  |  | |
| Number of PHASER\_IN/PHASER\_IN\_PHYs | 0 | 16 | 0% |  | |
| Number of PHASER\_OUT/PHASER\_OUT\_PHYs | 0 | 16 | 0% |  | |
| Number of BSCANs | 0 | 4 | 0% |  | |
| Number of BUFHCEs | 0 | 72 | 0% |  | |
| Number of BUFRs | 0 | 16 | 0% |  | |
| Number of CAPTUREs | 0 | 1 | 0% |  | |
| Number of DNA\_PORTs | 0 | 1 | 0% |  | |
| Number of DSP48E1s | 10 | 220 | 4% |  | |
| Number of EFUSE\_USRs | 0 | 1 | 0% |  | |
| Number of FRAME\_ECCs | 0 | 1 | 0% |  | |
| Number of ICAPs | 0 | 2 | 0% |  | |
| Number of IDELAYCTRLs | 0 | 4 | 0% |  | |
| Number of IN\_FIFOs | 0 | 16 | 0% |  | |
| Number of MMCME2\_ADVs | 0 | 4 | 0% |  | |
| Number of OUT\_FIFOs | 0 | 16 | 0% |  | |
| Number of PHASER\_REFs | 0 | 4 | 0% |  | |
| Number of PHY\_CONTROLs | 0 | 4 | 0% |  | |
| Number of PLLE2\_ADVs | 0 | 4 | 0% |  | |
| Number of PS7s | 1 | 1 | 100% |  | |
| Number of STARTUPs | 0 | 1 | 0% |  | |
| Number of XADCs | 0 | 1 | 0% |  | |
| Average Fanout of Non-Clock Nets | 4.12 |  |  |  | |

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| **Performance Summary** | | | | **[-]** |
| **Final Timing Score:** | 1345580 (Setup: 1345580, Hold: 0, Component Switching Limit: 0) | **Pinout Data:** | Pinout Report | |
| **Routing Results:** | All Signals Completely Routed | **Clock Data:** | Clock Report | |
| **Timing Constraints:** | **X** 1 Failing Constraint |  |  | |

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| **Detailed Reports** | | | | | | **[-]** |
| **Report Name** | **Status** | **Generated** | **Errors** | **Warnings** | **Infos** | |
| Translation Report | Current | Wed 14. Oct 22:58:17 2015 | 0 | 131 Warnings (0 new) | 3 Infos (0 new) | |
| Map Report | Current | Wed 14. Oct 23:05:37 2015 |  |  |  | |
| Place and Route Report | Current | Wed 14. Oct 23:09:15 2015 | 0 | 122 Warnings (0 new) | 2 Infos (0 new) | |
| Post-PAR Static Timing Report | Current | Wed 14. Oct 23:10:19 2015 | 0 | 0 | 4 Infos (0 new) | |
| Bitgen Report | Current | Wed 14. Oct 23:12:26 2015 | 0 | 119 Warnings (0 new) | 0 | |

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| **Secondary Reports** | | | **[-]** |
| **Report Name** | **Status** | **Generated** | |
| WebTalk Report | Current | Wed 14. Oct 23:12:44 2015 | |
| WebTalk Log File | Current | Wed 14. Oct 23:13:02 2015 | |

**Date Generated:** 10/14/2015 - 23:34:01